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Intrinsic Josephson junctions: integrated circuits and possible applications

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Abstract
With a novel double-sided fabrication method, stacks of intrinsic Josephson junctions (IJJs) superconductively connected to each other can be patterned and integrated with other circuits. On a slice of $Bi_2Sr_2CaCu_2O_{8+x}$ (BSCCO) 200–300 nm thick, over an area of $500 \times 420\ \mu m^2$, so far we are able to fabricate up to 2500 stacks. A single stack with submicrometre lateral sizes has already been obtained without observable degradation. Zero-crossing and non-zero-crossing Shapiro steps have been observed under irradiation from a far-infrared laser. Thus, quite a few good electronic devices can be built based on IJJs operated at relatively high temperatures and over a wide frequency range.

1. Introduction

In a high-T_C copper oxide superconductor, superconducting CuO_2 layers and non-superconducting layers along the c-axis form a one-dimensional array of intrinsic Josephson junctions (IJJs) at an atom scale if the a–b plane sizes are sufficiently small [1, 2]. To fabricate such junction stacks, mesa structures have been widely used since IJJs were discovered in 1992. However, some effects resulting from the interface between the IJJs in a mesa structure and the normal metal are undesirable. To avoid the problem, we should be able to fabricate a single stack of which the top and bottom electrodes are both superconducting. From the point of view of practical applications, a great number of junctions are often needed. For example, in a 1 or 10 V quantum voltage standard, a few thousands or a few tens of thousands of junctions in series are required to obtain Shapiro steps at sufficiently high voltages [3, 4]. Although we can easily include such a large number of junctions in one stack, this is certainly not a good choice because Joule heating or quasi-particle injection can drastically degrade or even damage the junctions [5, 6]. Thus, the compromise is to limit the junction number in a single stack in a well-controlled way, and at the same time to find a good way to connect many stacks together properly.

Bearing in mind the importance of solving the aforementioned problems, we have been working on developing a fairly ideal fabrication method using high-temperature superconducting single crystals. In fact, as reported earlier [7, 8], using a double-sided process we have been able to fabricate one-dimensional (1D), two-dimensional (2D) and three-dimensional (3D) arrays of IJJs which are singled out from inside a $Bi_2Sr_2CaCu_2O_{8+x}$ (BiSrCaCuO-2212, or BSCCO) single crystal. As this method provides access to the stack from both ends, it is relatively straightforward to integrate some additional circuits. The IJJs as well as the stacks are quite uniform regarding the direct current (dc) transport properties. Zero-crossing Shapiro steps at 760 GHz also have been shown in a four-stack array.

In this paper, we report on our latest experimental observations of zero-crossing Shapiro steps which appear up to 2.4 V in a 256-stack array. Also reported are non-zero-crossing Shapiro steps observable above liquid nitrogen temperature. In addition, the successful fabrication of an array containing 2500 stacks over an area of $500 \times 420\ \mu m^2$ is so encouraging that we think it is possible to use high-T_C IJJs for dc and programmable voltage standards. It turns out that our double-sided fabrication method can produce uniform junctions,

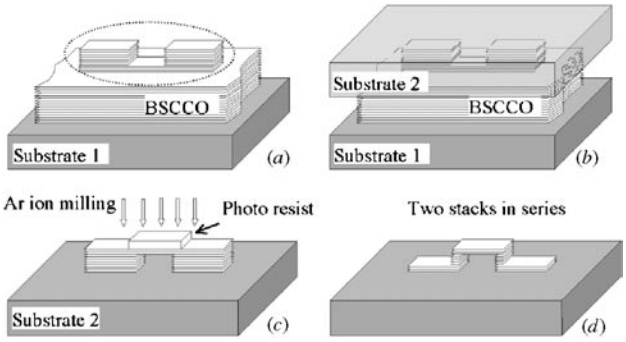

Figure 1. A schematic view of the double-sided fabrication process. While many kinds of substrates can be used for substrate 1, we use Si or MgO as substrate 2 for reducing high-frequency loss in the substrate.

large-scale arrays and submicrometre samples without observable degradation.

2. Fabrication and characterization

2.1. Fabrication of a 2500-stack array

The fabrication process was developed for fabricating a single stack earlier in 2001 [7], and adopted for fabricating an array of multiple stacks connected in series [8]. To begin with, a piece of BSCCO single crystal is cleaved, fixed on substrate 1, and plated with gold (figure 1(*a*)). A mesa with two stacks (marked by a dashed circle in the figure) is photolithographically patterned and fabricated. A very important step is to glue the top side of the mesa on to a second substrate (substrate 2 in figure 1(*b*)). Cleaving it from the big pedestal results in a Π-shaped sample about 200–300 nm thick standing on substrate 2. After sputtering 50 nm gold on to the sample, we put a photoresist strip on top of it to protect the central part (figure 1(*c*)). Argon ion milling is used to etch the rest of it down to a certain depth as required by the desired junction number (from a few to a few tens of nanometres, figure 1(*d*)). In principle, we can choose any preferred material for supporting this array. However, for high frequency applications, we often use Si or MgO as substrate 2 considering their low radio-frequency (rf) losses.

Figure 2 shows an optical microscope photograph of an array of 2500 BSCCO IJJs stacks on a MgO substrate. The transparent substrate makes it possible to take the photograph with back-side illumination. The *a–b* plane size of all stacks is designed to be $4 \times 4\ \mu m^2$. Also shown is the schematic view of four stacks in series. The Π-shaped structure shown in figures 1 and 2 is actually a 'building block' of the array. In fact, 1251.5 Π 'building blocks' can be found in figure 2. In addition to the 2500 series stacks, a single stack (marked A) and a pair of stacks (marked B) are also fabricated on the same chip for controlling the junction number in one stack and for detailed studies of the junction properties.

Attempting to measure the dc current–voltage (*I–V*) characteristics of the 2500-stack array, we realize that a bias of about 2000 V is needed to trace all the branches. Due to the technical impracticality, we use a bias whose maximum output is only 17 V for the measurements, implying that only about 700 junctions can be traced. To demonstrate the uniformity of

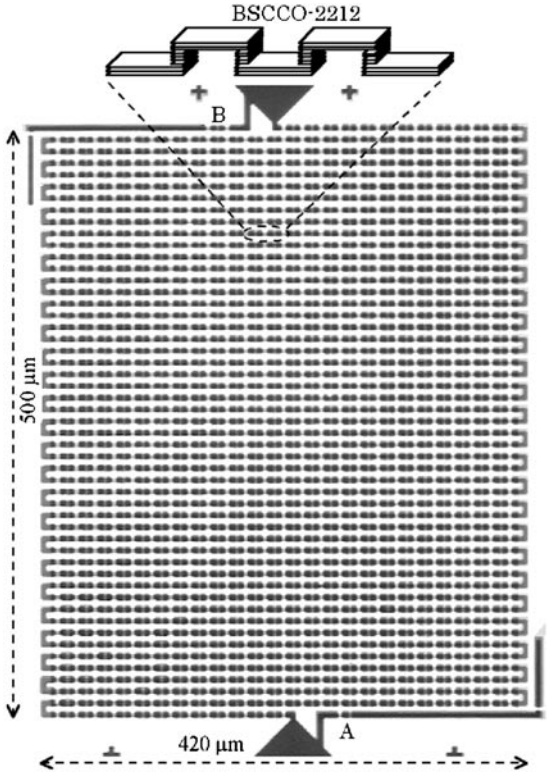

Figure 2. An optical photograph of an array of 2500 BSCCO IJJ stacks on a MgO substrate taken through an optical microscope with back-side illumination. Also shown is a schematic view of four stacks in series.

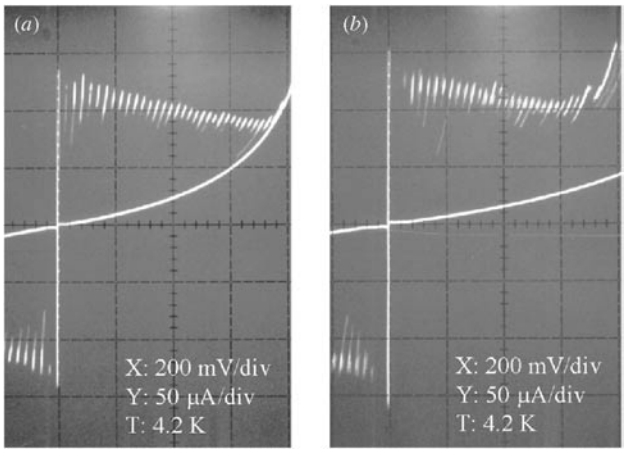

Figure 3. *I–V* characteristics of the stacks at (*a*) point A and (*b*) point B in figure 2. From this, we can find the junction number and the critical current for each stack.

the junction number (n) and the critical current (I_c) of different stacks, we measure the *I–V* curves of the single stack A or the pair of stacks B respectively. As shown in figure 3, the typical parameters of a sample are $n^{(A)} = 32, n^{(B)} = 30, I^A_{(c)} = 140\ \mu$A, and $I_c^{(B)} = 160\ \mu$A, where A and B denote the stack at point A, and one of the two stacks at point B. According to our experience, the difference of I_c is mainly caused by the different *a–b* plane size due to the misalignment during photolithography. The number difference can be attributed either to some steps on the surface of the cleaved single

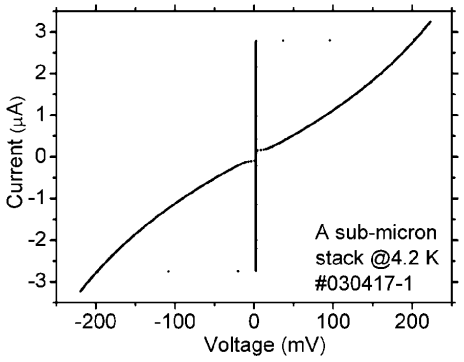

Figure 4. *I–V* characteristics of a submicrometre stack with 12 junctions inside.

crystal or to a shadow effect during the argon ion milling. Nevertheless, these problems are not intrinsic and can certainly be solved in future fabrication processes. We note that a clear and gradual decrease of critical currents appears when the stacks are at their voltage states in figure 3. This indicates that the more junctions that are in their voltage state, the smaller the critical current is. In other words, the critical current is rather sensitive to how many junctions are in the resistive state. This is consistent with earlier observations, which attributed these phenomena to quasi-particle injection and Joule heating [5, 6]. We can expect that the suppression of critical current and energy gap becomes more serious when the junction number is further increased, indicating that it is necessary to reduce the number of junctions in one stack, i.e. to fabricate stacks in series to include more junctions in the array.

Within each stack the measured number of junctions is about 31. Thus, we estimate that the array contains about 78 000 junctions altogether over an area of about 500 × 420 μm^2, i.e. the degree of integration is considerably high. Surely it is easy to include more junctions on one chip.

2.2. Fabrication of a submicrometre single stack

A scanning electron microscope equipped with a lithography system (LEO730, Raith Elphy) was employed to obtain submicrometre patterns as well as to improve the alignment. As the cleaved single crystal is only a few hundred nanometres thick, fast electrons can penetrate deep into the whole single crystal. Therefore, the secondary electron image is quite clear. For this reason, the patterns in different fabrication steps can be very well aligned.

Figure 4 shows the *I–V* curve of a stack with a lateral size of 0.5 × 0.5 μm^2. At a critical current of about 2.8 μA, all junctions switch to their voltage state simultaneously, indicating a perfect uniformity of all junctions in the stack. Further measurements show 12 junctions involved in the stack. The critical current density is about 1.1 kA cm^{-2}, which is a typical value of our single crystals. Therefore, there is no observable degradation during fabrication, even for samples with submicrometre size.

3. Terahertz response and possible applications

The IJJs fabricated in our experiments usually yield a T_C of about 90 K, the same as that of bulk single crystals. Therefore, the IJJs can be operated over a very wide temperature range. In our earlier work [8, 9], we confined ourselves to the observation of terahertz response at rather low temperatures at which the IJJs were highly hysteretic. In fact, Shapiro steps can also be observed up to temperatures very near T_c, revealing interesting features suitable for different applications at higher temperatures.

3.1. Zero-crossing Shapiro steps at low temperatures

In our earlier experiments, with irradiation at 1.6 THz, the heights of zero-crossing Shapiro steps were not very large and it seemed difficult to bias the stack on the step. Thus, it was very interesting to find whether or not we could obtain much larger steps to make possible some practical applications. So, we tested the response at a relatively low frequency of 760 GHz using the same cryostat and a far-infrared laser (FIR).

Samples with one, four and 256 stacks have been measured. As shown in figure 5(*a*), in the case of a single stack of 18 junctions, we can observe 18 sharp and large zero-crossing Shapiro steps spaced at 1.57 mV, satisfying the well-known Josephson frequency–voltage relation for irradiation at 760 GHz. The observed zero-crossing steps are actually the first-order Shapiro steps of each junction in the stack, i.e., the number of zero-crossing steps is equal to the number of junctions which are biased at their resistive states and irradiated with FIR power.

In the case of an array of four stacks, aligned along one line and involving about 116 junctions, we can observe zero-crossing steps up to voltages close to 0.18 V, indicating that most of the junctions contribute a voltage of 1.57 mV under 760 GHz irradiation. In figure 5(*b*), we can clearly see that all steps are vertical and with constant voltage intervals.

In the 256-stack array, there are about 11 000 junctions according to our design and measurement. As shown in figure 5(*c*), zero-crossing steps are observed up to voltages of 2.4 V, indicating that about 1500 junctions in the array are contributing. Obviously, this number is much less than 11 000. This raises the question about how many junctions in the array are contributing, and whether or not the corresponding Shapiro steps are zero-crossing. According to our design, with irradiation at 760 GHz, if each junction contributes a voltage of 1.57 mV, the highest voltage up to which Shapiro steps are observable will be 17 V, according to the Josephson frequency–voltage relation. There is at least one reason for the absence of zero-crossing steps at the expected voltages, i.e. the coupling between the FIR signal and the stacks has to be optimized. Although in every sample a bow-tie antenna has been integrated with the stacks, when more stacks are included and then the distance between the two elements of the antenna becomes larger, the gain of the antenna must be poorer. As a matter of fact, in the measurements on the 256-stack array, there is large scattering of step heights, reflecting the inhomogeneity of power distribution in different stacks. A multi-branch feeding structure similar to those used in niobium-based quantum voltage standards might be helpful in this regard [3, 4].

Compared to the well-developed low-T_C dc voltage standards, a few advantages can be found: (1) high operation temperatures, as we have observed zero-crossing steps up to

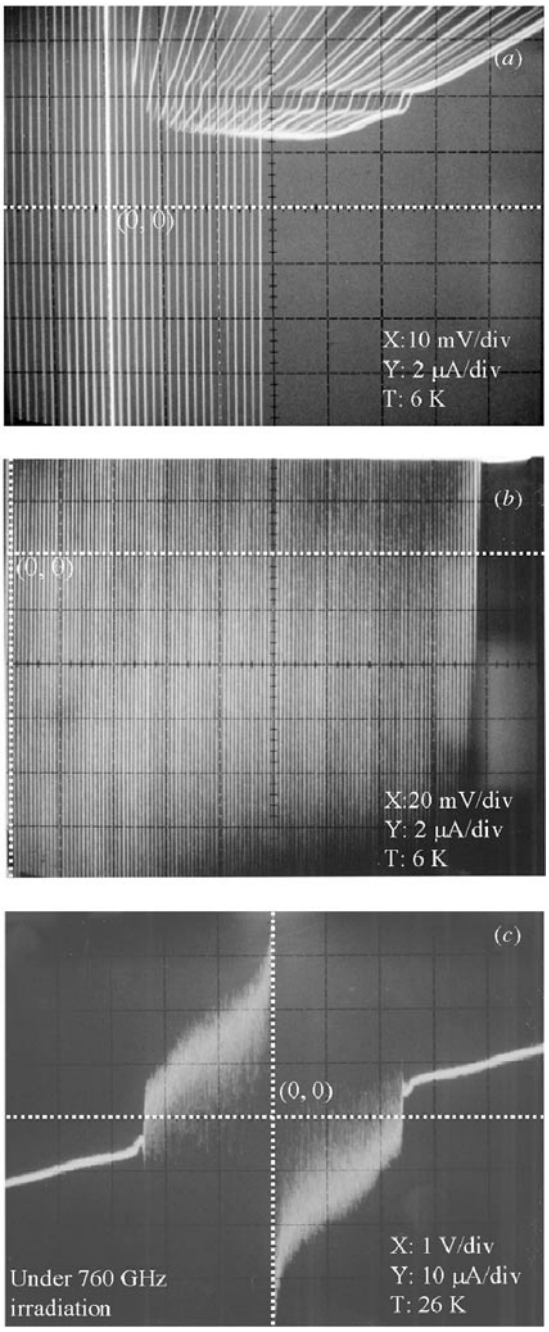

Figure 5. Zero-crossing Shapiro steps under irradiation at 760 GHz: (*a*) single stack with 18 junctions; (*b*) four stacks with about 116 junctions; (*c*) 256 stacks with about 11 000 junctions.

temperatures near 50 K; (2) high density of junctions due to naturally compact atomic scale, which may simplify the instrumentation significantly. As a matter of fact, stacked Nb-based tunnel junctions have been explored for the same reason [10, 11].

3.2. Non-zero-crossing Shapiro steps at liquid nitrogen temperatures

Figure 6 shows the typical *I–V* curve of a single stack operated at 84 K. Here the hysteresis, the voltage jumps, as well as the energy gaps of all junctions are suppressed. Locating at a

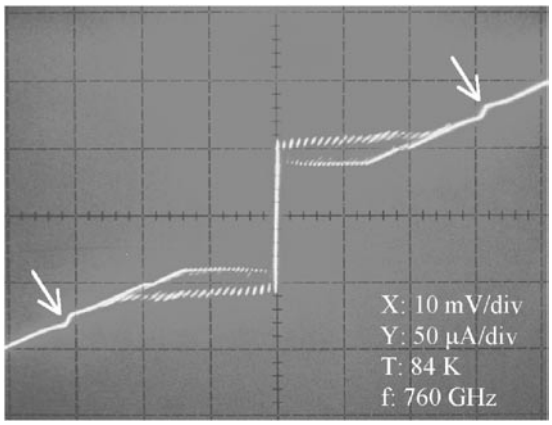

Figure 6. A Shapiro step observed in a single stack operated at 84 K.

voltage far away from the hysteresis region with 20 branches, a step can be found at about 32 mV. This step is actually the superposition of the first-order Shapiro steps in 20 junctions. In other words, biasing the stack to about 75 μA, we can have a quantized voltage which is determined only by the irradiation frequency and the known junction number. Provided that all stacks on one chip can have the same junction number, we can find applications of IJJs in programmable voltage standards according to the proposal by Hamilton *et al* [12]. The binary sequence of shunted Nb junction arrays can be replaced by a binary sequence of stacks of IJJs. Moreover, the D/A converter can be operated at liquid nitrogen temperatures.

For practical applications making use of zero-crossing or non-zero-crossing Shapiro steps, signal sources at lower frequencies are often preferred, i.e., sources at millimetre or centimetre wavebands. However, the response of IJJs to such 'low-frequency' sources can be chaotic because their plasma frequencies are usually a few hundred gigahertz [9], remarkably higher than those of the signal sources. Therefore, reducing the critical current density but maintaining the T_c will be a key step towards practical applications.

4. Conclusion

Using a double-sided fabrication method recently developed, 3D arrays of IJJs in BSCCO single crystals are realized. Zero-crossing and non-zero-crossing steps are observed, indicating a high potential for practical applications such as dc or programmable quantum voltage standards. It is essential to optimize the coupling between the array and the high-frequency signal source, and to improve the homogeneity of the power distribution between each junction. From the point of view of practical applications, it is also helpful if we can reduce the plasma frequency of the IJJs. As all of these problems appear to be solved, the demonstration of a very compact high-temperature Josephson voltage standard seems to be feasible.

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